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CRACKSTOP WITH RELEASE LAYER FOR CRACK CONTROL IN SEMICONDUCTORS

Abstract

Methods of forming and the integrated circuit device structure formed having vertical interfaces adjacent an existing crack stop around a perimeter of a chip, whereby the vertical interface controls cracks generated during side processing of the device such as dicing, and in service from penetrating the crack stop. The vertical interface is comprised of a material that prevents cracks from damaging the crack stop by deflecting cracks away from penetrating the crack stop, or by absorbing the generated crack energies. Alternatively, the vertical interface may be a material that allows advancing cracks to lose enough energy such that they become incapable of penetrating the crack stop. The present vertical interfaces can be implemented in a number of ways such as, vertical spacers of release material, vertical trenches of release material or vertical channels of the release material.